User's Guide
SLVU127–February 2005

TPS54073EVM-098 14-Amp, SWIFT™ Regulator Evaluation Module

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1 Introduction

This user's guide contains background information for the TPS54073 as well as support documentation for the TPS54073EVM-098 evaluation module (HPA098). The TPS54073EVM-098 performance specifications are given, as well as the schematic and bill of materials for the TPS54073EVM-098.

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1.1 Background

The TPS54073 dc/dc converter is designed to provide up to 14 A output from an input voltage source of 2.2 V to 4.0 V. This device features Disabled Sink During Startup (DSDS) and is intended for use in applications where the output may be pre-charged. At start up, the TPS54073 ramps up to the desired set point from the initial pre-charge voltage without first discharging the output to ground. Rated input voltage and output current range is given in Table 1. This evaluation module is designed to demonstrate the small PCB areas that may be achieved when designing with the TPS54073 regulator, and does not reflect the high efficiencies that may be achieved when designing with this part. The switching frequency is set at a nominal 700 kHz, allowing the use of a small-footprint 2.2-µH output inductor. The high and low-side MOSFETs are incorporated inside the TPS54073 package along with the gate drive circuitry. The low drain-to-source on resistance of the MOSFETs allows the TPS54073 to achieve high efficiencies and helps to keep the junction temperature low at high output currents. The compensation components are provided external to the IC, and allow for an adjustable output voltage and a customizable loop response. Additionally, the TPS54073 provides a full feature set including programmable undervoltage lockout, sychronization, adjustable switching frequency, enable, and power-good functions

Table 1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54073EVM-098	VIN = 3.0 V to 4.0 V, PVIN = 2.2 V to 4.0 V	0 A to 14 A

1.2 Performance Specification Summary

A summary of the TPS54073EVM-098 performance specifications is provided in Table 2. Specifications are given for an input voltage of PVIN = VIN = 3.3 V and an output voltage of 1.5 V unless otherwise specified. The TPS54073EVM-098 is designed and tested for PVIN = 2.2 V to 4.0 V. The ambient temperature is 25°C for all measurements, unless otherwise noted. The maximum input voltage for the TPS54073 is 4.0 V.

Table 2. TPS54073EVM-098 Performance Specification Summary

SPECIFICATION		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PVIN voltage range			2.2	3.3	4.0	V
VIN voltage range				3.3		V
Output voltage set point				1.5		V
Output current range		V_{IN} = 3.3 V	0		14	A
Line regulation		I_O = 0 A – 14 A, PVIN = 2.2 V - 4.0 V, VIN = 3.3 V		±0.2%		
Load regulation		VIN = PVIN = 3.3 V, I_O = 0 A to 3 A		±0.2%		
Load transient response	Voltage change	I_O = 3.5 A to 10.5 A		–175		mV
	Recovery time			250		ms
	Voltage change	I_O = 10.5 A to 3.5 A		175		mV
	Recovery time			250		ms
Loop bandwidth		PVIN = 2.2 V		30		kHz
		PVIN = 4.0 V		45		
Phase margin		PVIN = 2.2 V		65		°
		PVIN = 4.0 V		52		
Input ripple voltage				300	350	mVpp
Output ripple voltage				8	15	mVpp
Output rise time				N/A		ms
Operating frequency				700		kHz
Max efficiency		PVIN=VIN = 3.3 V, V_O = 1.5 V, I_O = 2.0 A		92%		

1.3 Modifications

While the TPS54073EVM-098 is designed to demonstrate the small size that can be attained when designing with the TPS54073, many features allowing extensive modifications have been included in this EVM.

1.3.1 Output Voltage Setpoint

To change the output voltage of the EVM, it is necessary to change the value of resistor R2. Changing the value of R2 can change the output voltage in the range of 0.9 V to 2.5 V. The value of R2 for a specific output voltage can be calculated using Equation 1.

$$R2 = 10\ k\Omega \times \frac{0.891\ V}{V_O - 0.891\ V} \quad (1)$$

Table 3 list the R2 values for some common output voltages. Note that PVIN must be greater than 3 V to generate a 2.5 V output.

Table 3. Output Voltages Available

Output Voltage (V)	R_2 Value (Ω)
1.0	82.3 k
1.2	28.7 k
1.5	14.7 k
1.8	9.76 k
2.5	5.49 k

1.3.2 Switchng Frequency

The switching frequency of the EVM is set to 700 kHz by setting R4 to 71.5 kΩ. The switching frequency may be trimmed to any value between 280 kHz and 700 kHz by changing the value of R4 using Equation 2. The EVM may also be set to one of the two internally-programmed frequencies. Remove R4 and use a jumper on the three-pin header J4 to select 350-kHz or 550-kHz operation. The jumper settings are conveniently silk-screened on the EVM printed circuit board. Note that decreasing the switching frequency will result in increased output ripple unless the value of L1 is increased.

$$f_{SW} = \frac{100\ k\Omega}{R2} \times 500(kHz) \quad (2)$$

1.3.3 Input Filter

An onboard electrolytic input capacitor is included at C1. Depending on the application, this capacitor may be removed.

1.3.4 Split Input Voltage Rails

The TPS54073 is provided with two input-voltage rails, PVIN and VIN. In normal operation, the two input voltages would be applied per Table 1 at the J1 and J2 connectors. It is possible to operate the EVM from a single 3.0-V to 4.0-V source by applying the voltage at connector J1, and installing a jumper on JP1.

1.3.5 Synchronization

The TPS54073EVM-098 may be synchronized to an external clock frequency. The synchronization-frequency range is 330 kHz to 700 kHz. Drive a synchronization signal into the SYNC pin by connecting to Pin 2 of J4, and use R4 to set the free-running frequency to 80% of the synchronization-signal frequency.

1.3.6 Extending Slow Start Time

The slow-start time may be extended by changing the value of C5. The value for C5 for a desired slow-start time is given by Equation 3.

$$C5(\mu F) = T_{SS}(ms) \times \frac{5\ \mu A}{1.2\ V} \quad (3)$$

1.3.7 Output Precharge

Connector J6 is provided to allow an external pre-charge voltage to be applied to the output. This voltage may be an external voltage source or possibly the PVIN voltage connected through series-connected diodes. It is important not to allow the pre-charge voltage to exceed the final set output voltage. The TPS54073 will not start up properly if the pre-charge level exceeds the output voltage.

2 Test Setup and Results

This chapter describes how to properly connect, setup, and use the TPS54073EVM-098 evaluation module. The chapter also includes test results typical for the TPS54073EVM-098 and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and startup.

2.1 Input / Output Connections

The TPS54073EVM-098 is provided with input/output connectors and testpoints as shown in Table 4. A power supply capable of supplying 12 A should be connected to J1 through a pair of 14 AWG wires. A power supply capable of supplying 25 mA should be connected to J2 through a pair of 22 AWG wires. The load should be connected to J3 through a pair of 14 AWG wires. The maximum load current capability should be 14 A. Wire lengths should be minimized to reduce losses in the wires. Testpoints TP1 and TP2 provide a place to monitor the the PVIN and VIN input voltages wth TPS providing a convenient ground reference. TP7 is used to monitor the output voltage with TP8 as the ground reference.

Table 4. EVM Connectors and Testpoints

Reference Designator	Function
J1	PVIN, 2.2 V to 4.0 V, 3.3 V nominal
J2	VIN, 3.3 V nominal, 3.0 to 4.0 V
J3	VOUT, 1.5 V at 14 A maximum
J4	3 pin header for VIN, SYNC and GND. With R4 open, jumper SYNC to VIN for 550 kHz operation or SYNC to GND for 350 kHz operation,
J5	2 pin header for ENA, ground to disable, open to enable
J6	Output voltage pre-charge connector
JP1	Jumper to connect VIN to PVIN
TP1	VIN test point at VIN connector
TP2	PVIN test point at PVIN connector
TP3	GND testpoint at VIN and PVIN connectors
TP4	PWRGD signal monitor testpoint
TP5	Test point used for loop response measurements
TP6	PH testpoint
TP7	Output voltage testpoint at VOUT connector
TP8	GND testpoint at VOUT connector

2.2 Efficiency

The TPS54073EVM-098 efficiency peaks at load current of about 2 A, and then decreases as the load current increases towards full load. Figure 1 shows the efficiency for theTPS54073 at an ambient temperature of 25°C. The efficiency is lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the MOSFETs. The efficiency is slightly lower at 700 kHz than at lower switching frequencies due to the gate and switching losses in the MOSFETs.

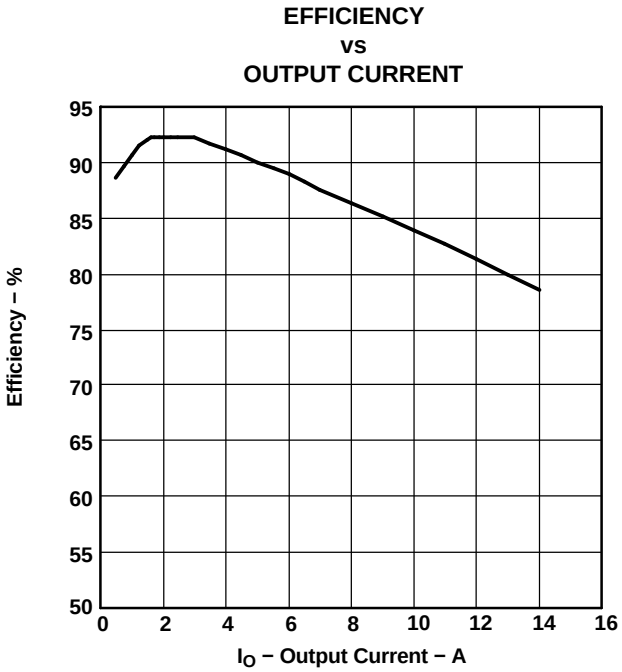

Figure 1. Measured Efficiency, TPS54073

2.3 Output Voltage Regulation

The output voltage load regulation of the TPS54073EVM-098 is shown in Figure 2, while the output voltage line regulation is shown in Figure 3. Measurements are given for an ambient temperature of 25°C.

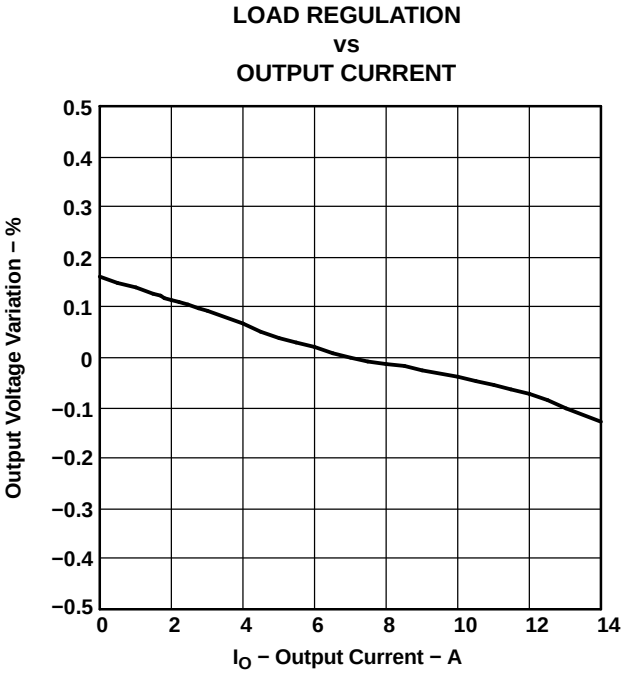

Figure 2. Load Regulation

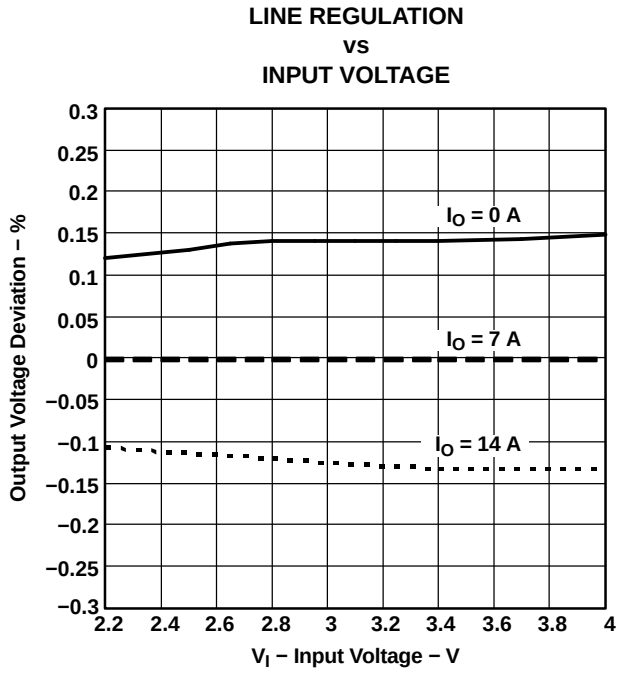

Figure 3. Line Regulation

2.4 Load Transients

The TPS54073EVM-098 response to load transients is shown in Figure 4. The current step is from 25 to 75 percent of maximum rated load. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

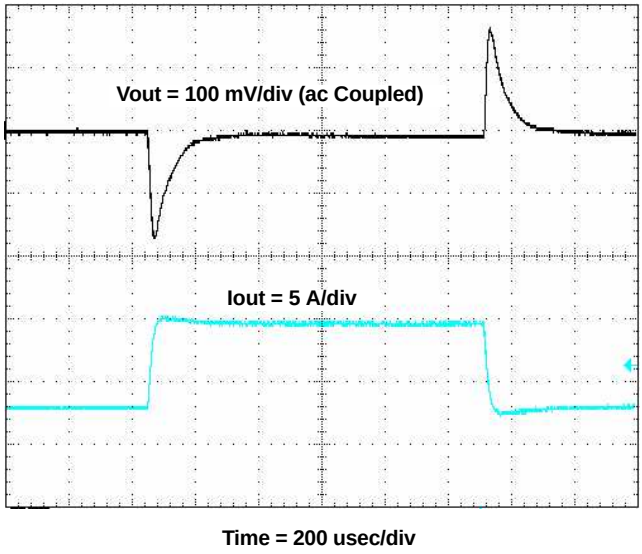

Figure 4. Load Transient Response, TPS54073

2.5 Loop Characteristics

The TPS54073EVM-098 loop-response characteristics are shown in Figure 5 and Figure 6. Gain and phase plots are shown for each device at PVIN voltages of 2.2 V and 4.0 V.

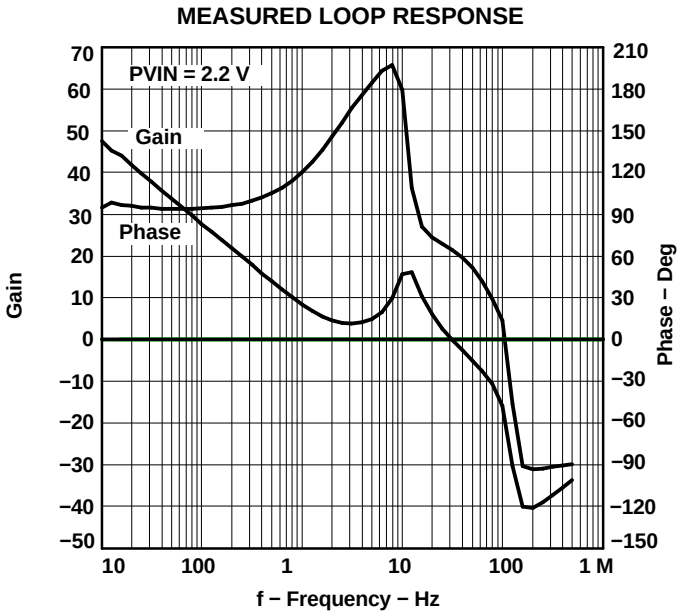

Figure 5. Measured Loop Response, TPS54073, PVIN = 2.2 V

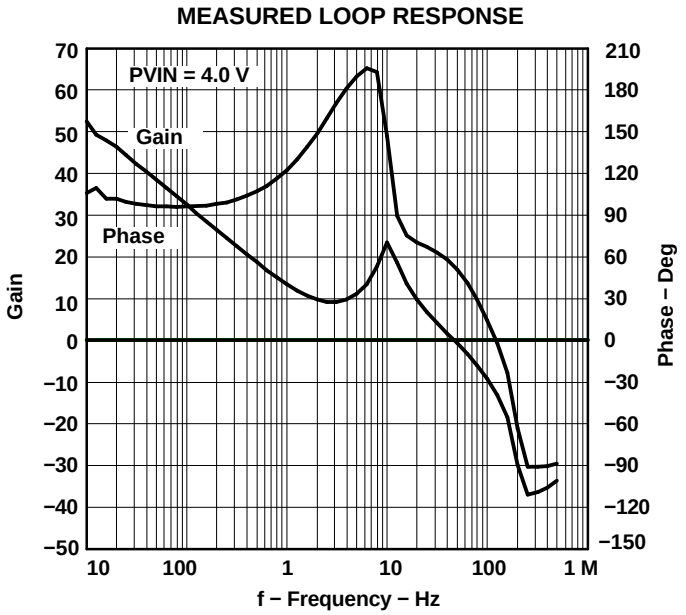

Figure 6. Measured Loop Response, TPS54073, PVIN = 4.0 V

2.6 Output Voltage Ripple

The TPS54073EVM-098 output voltage ripple is shown in Figure 7. The input voltages are PVIN = VIN = 3.3 V for the TPS54073. Output current is the rated full load of 14 A. Voltage is measured directly across output capacitors.

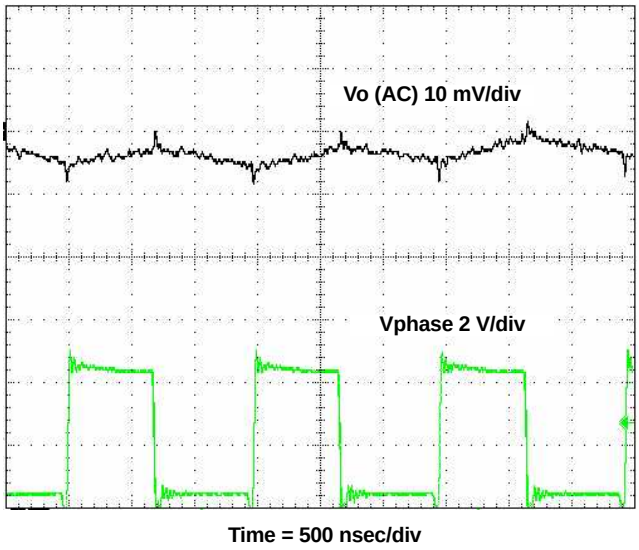

Figure 7. Measured Output Voltage Ripple, TPS54073

2.7 Input Voltage Ripple

The TPS5456EVM-058 output voltage ripple is shown in Figure 8. The input voltages PVIN = VIN = 3.3 V for the TPS54073. Output current for each device is at full rated load of 14 A.

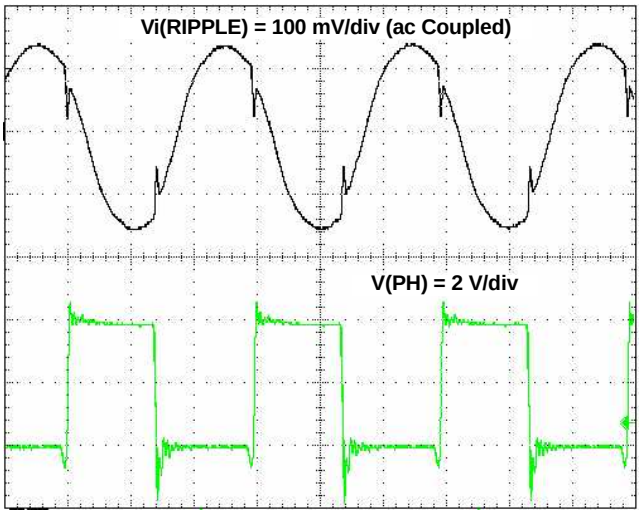

Figure 8. Input Voltage Ripple, TPS54073

2.8 Powering Up

The TPS54073EVM-098 start up waveforms are shown in Figure 9 and Figure 10. In Figure 9, the top trace shows PVIN and VIN, which are tied together, charging up from 0 V to 3.3 V. The output of the circuit is connected to the input with three Schottky diodes in series. As the input voltage rises, the output is precharged through the series diodes. When the input voltage reaches the internally set UVLO threshold voltage, the slow-start sequence begins. After a delay, the internal reference begins to ramp up linearly at the externally set slow start rate towards 0.891 V. When the internal ramp exceeds the fed-back portion of the pre-charged output at the VSENSE pin by a sufficient amount to command 100% duty cycle at the PWM comparator, switching begins. After a brief jump in the output voltage, the output ramps up linearly to the final value of 1.5 V. In Figure 10, the output voltage is shown relative to SS/ENA. PVIN and VIN are applied to the EVM while SS/ENA is held low, disabling the device. The output is again pre-charged using a single diode and an external 1.2 V source. When SS/ENA is released, the slow-start voltage begins to ramp up at the externally set rate. When the SS/ENA voltage reaches the enable-threshold votage of 1.2 V, the start-up sequence begins as described above.

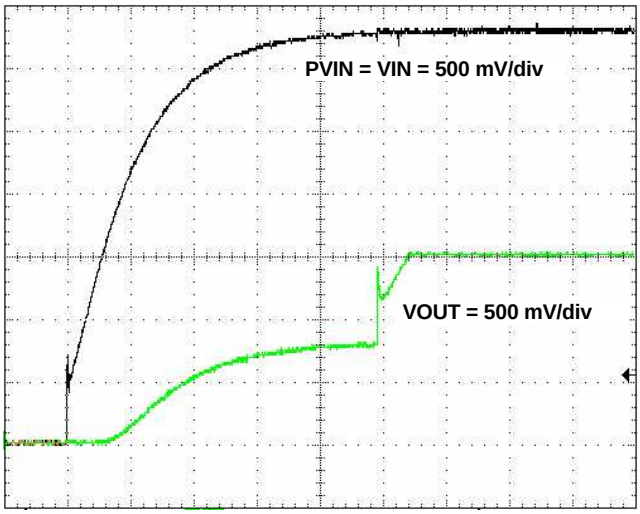

Figure 9. Power Up, VOUT relative to VIN

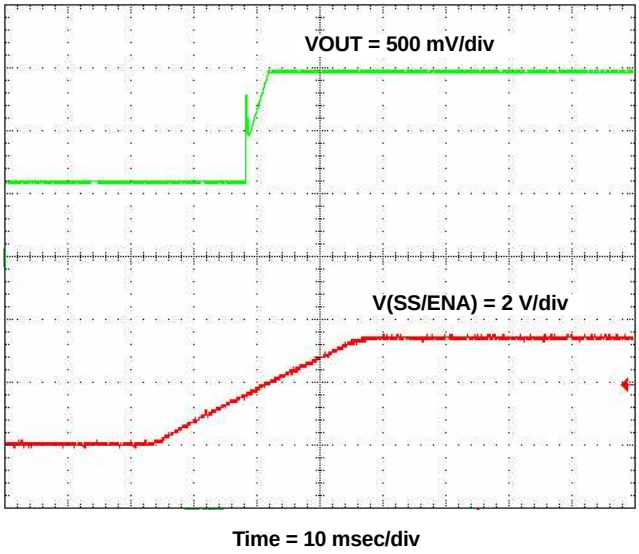

Figure 10. Power Up, VOUT relative to SS/ENA

3 Board Layout

This chapter provides a description of the TPS54073EVM-098 board layout and layer illustrations.

3.1 Layout

The board layout for the TPS54073EVM-098 is shown in Figure 11 through Figure 15. The topside layer of the TPS54073EVM-098 is laid out in a manner typical of a user application. The top, bottom and internal ground layers are 2.0 oz. copper.

The top layer contains the main power traces for VIN, VOUT, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54073 and a large area filled with ground. The bottom layer contains ground and VOUT copper areas, and some signal routing. The two internal layers are dedicated ground layers. The top and bottom and internal ground traces are connected with multiple vias placed around the board including 10 directly under the TPS54073 device to provide a thermal path from the PowerPAD land to ground.

The input decoupling capacitors (C1, C9, C10 and C11), bias decoupling capacitor (C4, and bootstrap capacitor (C3) are all located as close to the IC as possible. In addition, the compensation components are also kept close to the IC. The compensation circuit ties to the output voltage at the point of regulation, adjacent to the high frequency bypass output capacitor.

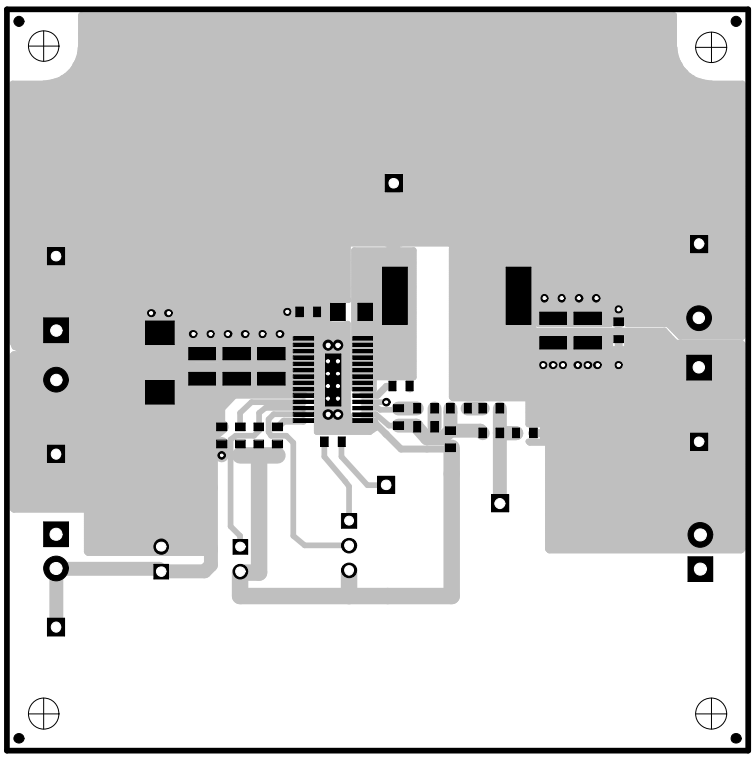

Figure 11. Top-side Layout

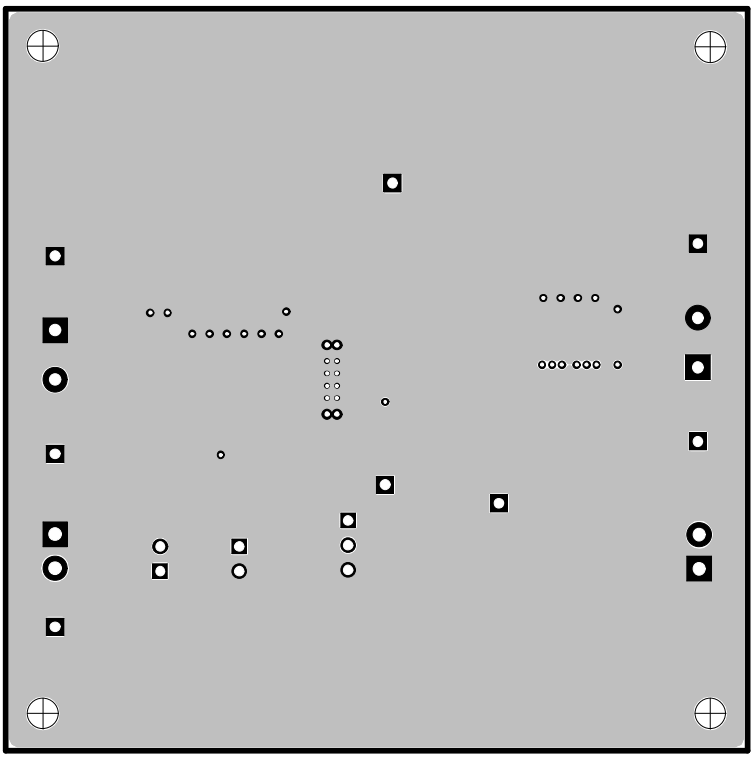

Figure 12. Internal Ground Layer 2

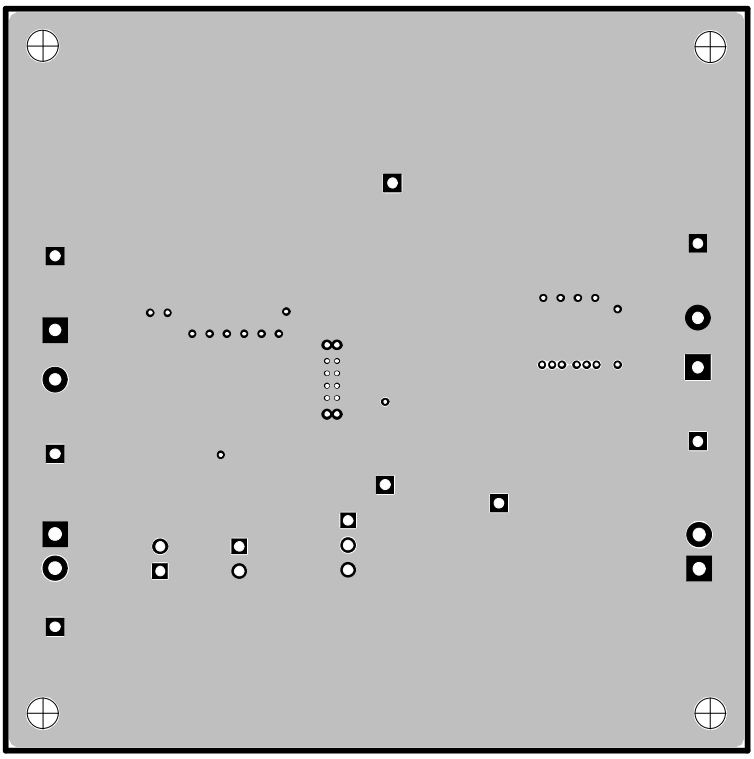

Figure 13. Internal Ground Layer 3

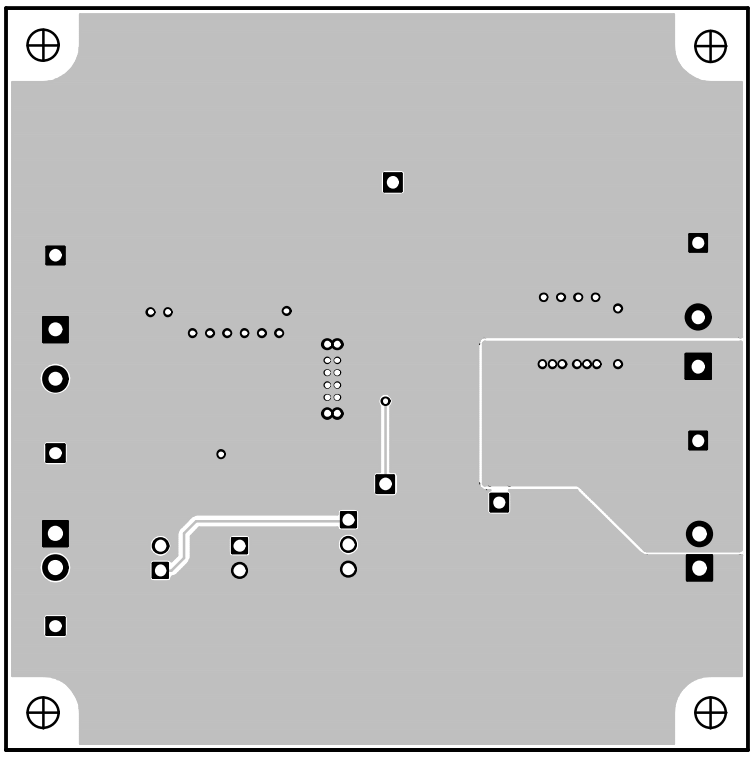

Figure 14. Bottom Side Layout (looking from top side)

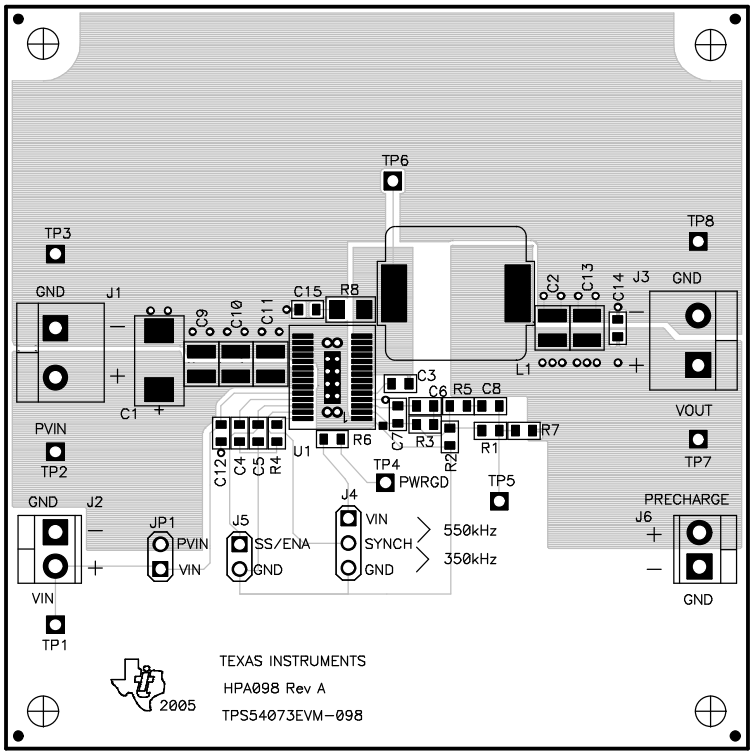

Figure 15. Top Side Assembly

4 Schematic and Bill of Materials

The TPS54073EVM-098 schematic and bill of materials are presented in this chapter.

4.1 Schematic

The schematic for the TPS54073EVM-098 is shown in Figure 16.

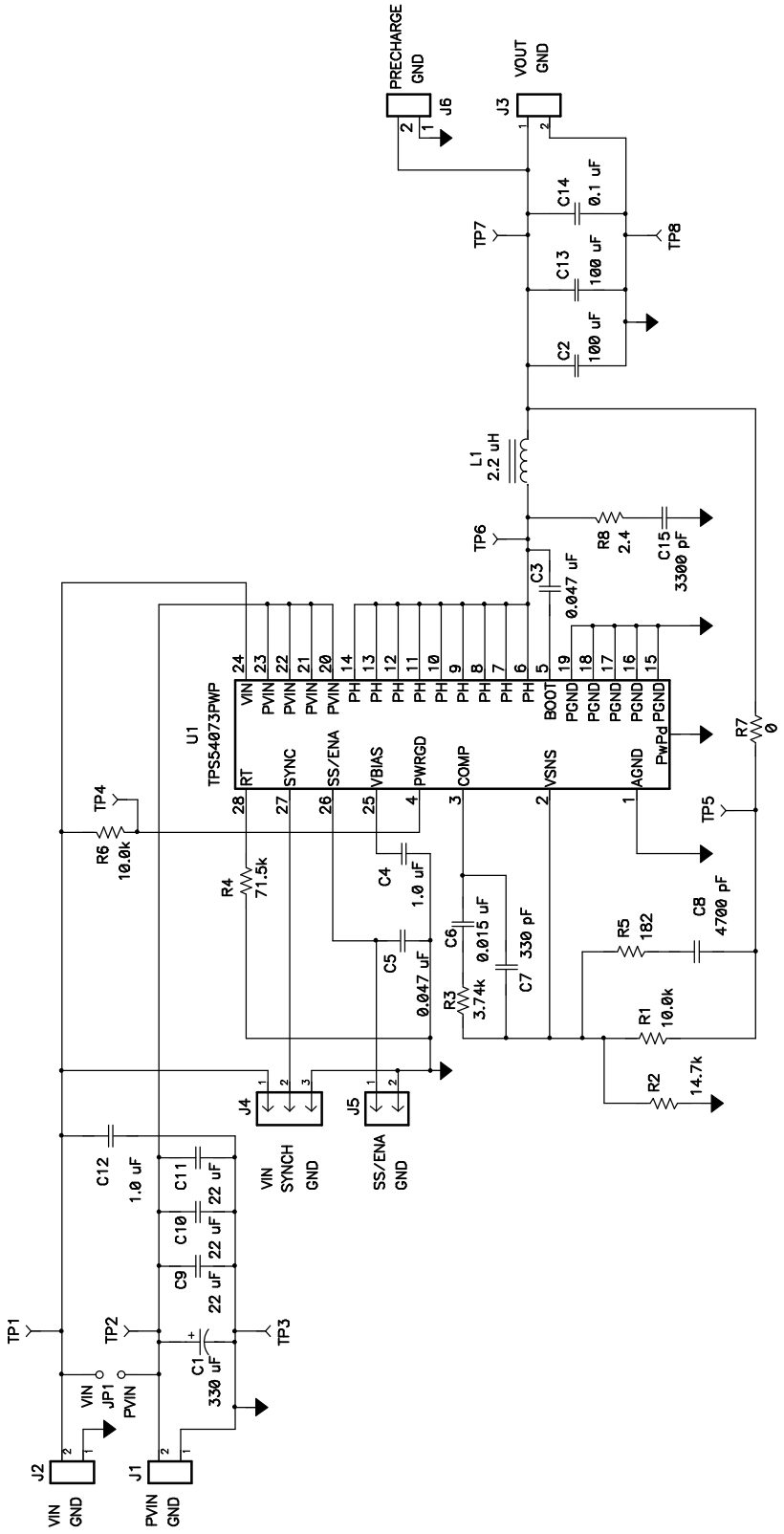

Figure 16. TPS54073EVM-098 Schematic

4.2 Bill of Materials

The bill of materials for the TPS54073EVM-098 is given by Table 5.

Table 5. TPS54073EVM-098 Bill of Materials

COUNT	REF DES	DESCRIPTION	SIZE	PART NUMBER	MFR
1	C1	Capacitor, POSCAP, 330 µF, 6.3-V, 10-mΩ, 20%	E Case	6TPD330M	Sanyo
1	C14	Capacitor, Ceramic, 0.1 µF, 16-V, X7R, 10%	0603	Std	Std
1	C15	Capacitor, Ceramic, 3300-pF, 50-V, X7R, 10%	0603	Std	Std
2	C2, C13	Capacitor, Ceramic, 100 µF, 6.3-V, X5R, 20% 1210		C3225X5R0J107M	TDK
2	C3, C5	Capacitor, Ceramic, 0.047 µF, 25-V, X7R, 10%	0603	Std	Std
2	C4, C12	Capacitor, Ceramic, 1.0 µF, 10-V, X5R, 10%	0603	Std	Std
1	C6	Capacitor, Ceramic, 0.015 µF, 50-V, X7R, 10%	0603	Std	Std
1	C7	Capacitor, Ceramic, 330-pF, 50-V, X7R, 10%	0603	Std	Std
1	C8	Capacitor, Ceramic, 4700 pF, 50-V, X7R, 10%	0603	Std	Std
3	C9, C10, C11	Capacitor, Ceramic, 22 µF, 16-V, X7R, 10%	1210	C3225X7R1C226KT	TDK
2	J1, J3	Terminal Block, 2-pin, 15-A, 5,1 mm	0.40 x 0.35	ED1609	OST
2	J2, J6	Terminal Block, 2-pin, 6-A, 3.5 mm	0.27 x 0.25	ED1514	OST
1	J4	Header, 3-pin, 100 mil spacing, (36-pin strip)	0.100 x 3	PTC36SAAN	Sullins
1	J5	Header, 2-pin, 100 mil spacing, (36-pin strip)	0.100 x 2	PTC36SAAN	Sullins
1	JP1	Header, 2-pin, 100 mil spacing, (36-pin strip)	0.100 x 2	PTC36SAAN IHLP5050CE-01	Sullins
1	L1	Inductor, SMT, 2.2 µH, 29-A, 8-milliohm	0.51 x 0.51	2R2	Vishay
2	R1, R6	Resistor, Chip, 10.0 kΩ, 1/16-W, 1%	0603	Std	Std
1	R2	Resistor, Chip, 14.7 kΩ, 1/16-W, 1%	0603	Std	Std
1	R3	Resistor, Chip, 3.74 kΩ, 1/16-W, 1%	0603	Std	Std
1	R4	Resistor, Chip, 71.5 kΩ, 1/16-W, 1%	0603	Std	Std
1	R5	Resistor, Chip, 182 Ω, 1/16-W, 1%	0603	Std	Std
1	R7	Resistor, Chip, 0 Ω, 1/16-W, 5%	0603	Std	Std
1	R8	Resistor, Chip, 2.4 Ω, 1/8-W, 1%	1206	Std	Std
6	TP1, TP2, TP4–TP7	Test Point, Red, 1 mm	0.038	240-345	Farnell
2	TP3, TP8	Test Point, Black, 1 mm	0.038	240-333	Farnell
1	U1	IC, 2.2V-4V, 13A O/P Synchronous Buck PWM Switch (SWIFT)	PWP28	TPS54073PWP	TI
1		PCB, 3 In x 3 In x 0.062 In		HPA098	Any
1		Shunt, 100-mil, Black	0.100	929950-00	3M

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